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# Fpga Implementation of Truncated Multiplier Using Reversible Logic Gates

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***ABSTRACT:*** *Multiplication is a major building block of Digital Signal Processing applications. The truncated multiplier has shown much more reduction in device utilization as compared to standard multiplier. The basic idea of this technique is to discard some of least significant partial products and to introduce compensation circuit to reduce approximation error. Thus area and power consumption of the arithmetic unit are significantly reduced, which also decreases the delay. In addition to this power consumption can be reduced using reversible logic gate. It has been shown that in any logic functions kT*log2 joules (where k is Boltzman's constant and T is the absolute temperature) of heat energy is dissipated per state transition. This loss can be reduced using reversible logic gate; in fact zero power dissipation can also be achieved. In this paper Trancated multiplier using reversible logic is implemented using 180nm CMOS technology which gives 19ns delay & 9.5uW power at 1Mhz.*

***KEY WORDS:*** *FPGA, Truncated multiplier, Reversible logic*

## I. INTRODUCTION

The advancement in higher-level integration and fabrication process has emerged in better logic circuits and energy loss has also been dramatically reduced over the last decades. This trend of reduction of heat in computation also has its physical limit according to Landauer, who proved that in logic computation every bit of information loss generates *kTln2 joules* [2] of heat energy, where *k* is Boltzmann's constant of $1.38x10^{-23} J/K$, and *T* is the absolute temperature of the environment. At room temperature, the dissipating heat is around 2.9 x $10^{-21}$ *J*. Energy loss by Landauer limit is important because it is likely that the growth of heat generation due to information loss will be noticeable in future. Bennett showed that zero energy dissipation would be possible if the network consists of reversible gates only. The Reversible adder circuits design which has combined advantages of less chip area, improved power dissipation and timing delay can be used as the building blocks in the design of reversible multipliers, arithmetic logic unit (ALU), successive approximation registers etc..

The three key factors in choosing an optimum multiplier for all DSP applications are *area, power & delay.* By parallel processing and pipelining a high speed multiplication can be achieved for DSP applications, this could be made more efficient by introducing truncated multiplication. The basic idea of this technique is to discard some of the least significant partial products and to introduce compensation circuit to reduce approximation error [10]. Thus area and power consumption of the arithmetic unit are significantly reduced, which also decreases the delay.

In this paper we are implementing a Truncated Multiplier using reversible logic gates [peres].Doing so we can reduce the power dissipation due to the rapid switching of internal signals. The paper is organized as follows. Section II presents an overview of Peres reversible logic gate & truncated multiplier. In Section III, we present the related work. Section 4 describes the FPGA implementation of the multiplier. Section 5 discusses the future improvements and section 6 concludes the paper.

## II. REVERSIBLE LOGIC

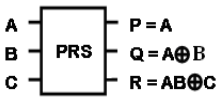
A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs.

Features for any gate to become reversible gate as follows[1]:

- Number of input and output lines must be the same.
- Feedback (loop) is not allowed in reversible logic.
- Fan-out is not allowed in reversible logic; Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.
- One of the major constraints in reversible logic is to minimize the number of reversible gates used.
- Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations. Garbage is the number of outputs added to make an n-input k-output Boolean function ((n,k)function) reversible
- Using minimum number of input constants.

There are many types of reversible logic gates currently being used .eg fennyman gate, toffoli gate, peres gate etc. For our implementation we have used Peres reversible logic gate.

Peres gate:




**Truncated multiplier:**

Consider a 6 x 6 bit multiplication:


**Figure 2.1: 6x6 standard multiplier**

As shown above, the LSB computation is not done in a truncated multiplier. Multiplication and squaring functions are used extensively in applications such as DSP, image processing and multimedia. Here if use truncated multipliers instead of parallel multipliers the power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also reduces.

The circuit for a truncated multiplier constructed using full adders is as shown below:

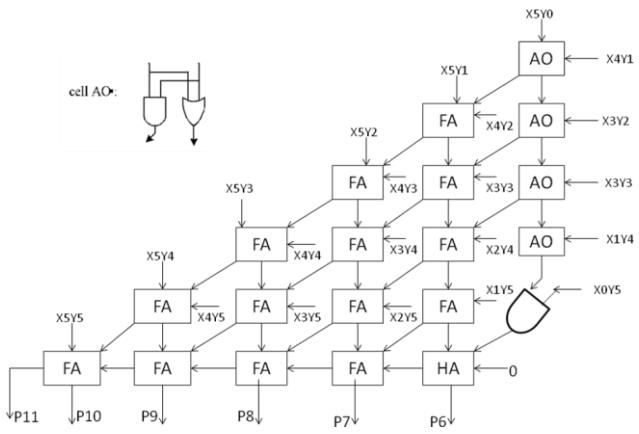



**Figure 2.2: 6x6 Truncated multiplier**

## III. DESIGN OF TRUNCATED MULTIPLIER USING PERES REVERSIBLE LOGIC GATE

The first step is the design of half adder & full adder using peres gate as shown below:

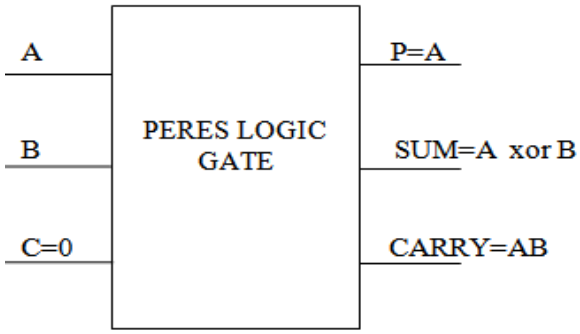



Figure 3.1: half adder using peres gate

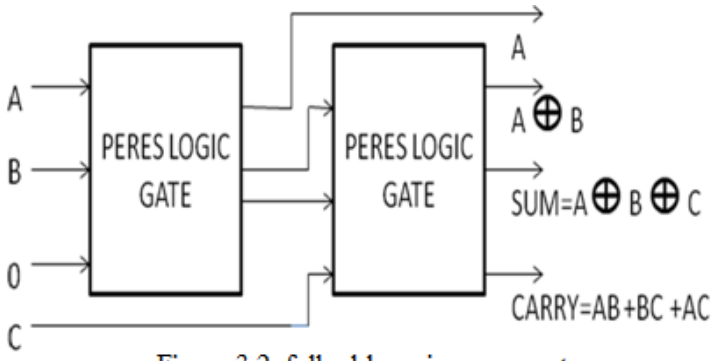
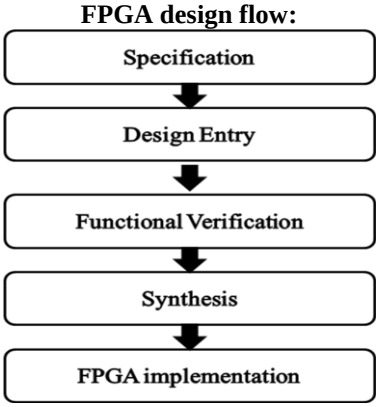



Figure 3.2: full adder using peres gate

## IV. FPGA IMPLEMENTATION

FPGAs are an ideal platform for the implementation of computationally intensive and massively parallel architecture as they are parallel in nature and have high frequency. Also FPGAs have advantage of reconfigurability speed and flexibility in software compared to high cost non reconfigurable ASICs. Here we have used Spartan -3 which belongs to the fifth generation Xilinx family. It is specifically designed to meet three needs of high volume, low unit cost electronic systems. The family consists of eight member offering densities ranging from 50000 to five million system gates[9]. The Spartan -3 FPGA consists of five fundamental elements: CLB, IOBs, Block RAMs, dedicated multipliers and digital clock managers (DCMs), Figure 4.1 shows the FPGA implementation and Figure 4.2 shows Test bench waveform of design, Hardware Synthesis of Design has been carried out using cadence's RTL compiler to analyze the power and area consumption. The comparison details are show in table 1

**FPGA design flow:**



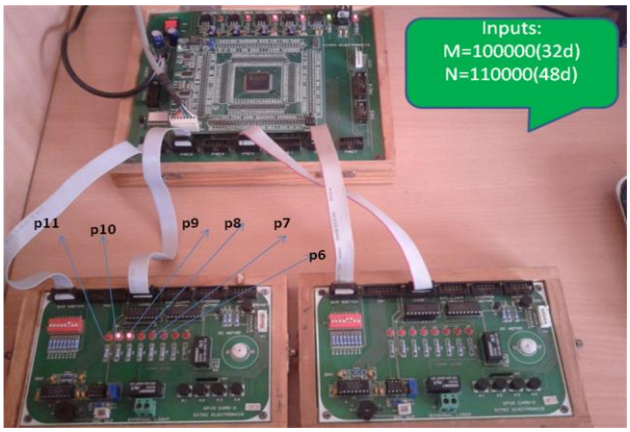



Figure 4.1 : FPGA implementation

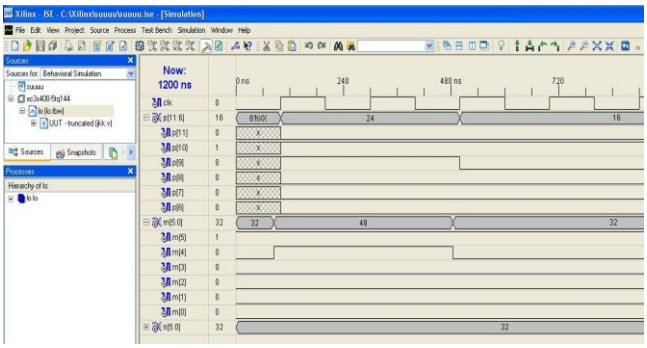


Figure 4.2: Test Bench Waveform of 6x6 truncated multiplier

Device utilization for multiplier

| | | | | |
|---|---|---|---|---|
| Number of Slices: | 23 | out of | 3584 | 0% |
| Number of 4 input LUTs: | 40 | out of | 7168 | 0% |
| Number of bonded IOBs: | 18 | out of | 97 | 18% |

| **Multiplier(6X6 bit)** | **AREA** | **POWER** |
|---|---|---|
| DADDA multiplier | 1009 $\mu m^2$ | 21131.386nW |
| Truncated Multiplier | 439$\mu m^2$ | 9554.2nW |

**Table 1: Synthesis report**

## V. CONCLUSION

In this paper we presented the design of truncated multiplier using peres reversible logic gate and its implementation on FPGA (Spartan-3) using VERILOG coding.

It was observed that the combinational path delay remained the same even with the use of reversible gates for the construction of the circuit, the two images are compared using normal multiplier and using truncated multiplier. its found that number of bits required for storage is very less compared to normal multiplication. The results shows the use of truncated multiplication for DSP application is encouraging.

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